DATA SHEET

74LVC257A
Quad 2-input multiplexer with 5 V tolerant inputs/outputs; 3-state

Product specification
2004 Jan 23
Supersedes data of 2003 Nov 17

Philips
Semiconductors

PHILIPS

Quad 2-input multiplexer with 5 V tolerant inputs/outputs; 3-state

74LVC257A

FEATURES

- 5 V tolerant inputs/outputs, for interfacing with 5 V logic
- Wide supply voltage range from 1.2 to 3.6 V
- CMOS low-power consumption
- Direct interface with TTL levels
- Output drive capability 50 Ω transmission lines at 85 °C
- Complies with JEDEC standard no. 8-1A
- ESD protection:
  HBM EIA/JESD22-A114-A exceeds 2000 V
  MM EIA/JESD22-A115-A exceeds 200 V
- Specified from –40 to +85 °C and –40 to +125 °C.

DESCRIPTION

The 74LVC257A is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 or 5.0 V devices. In 3-state operation, outputs can handle 5 V. This feature allows the use of these devices as translators in a mixed 3.3 and 5 V environment.

The 74LVC257A is a quad 2-input multiplexer with 3-state outputs, which select 4 bits of data from two sources and are controlled by a common data select input (pin S). The data inputs from source 0 (pins 1I0 to 4I0) are selected when pin S is LOW and the data inputs from source 1 (pins 1I1 to 4I1) are selected when pin S is HIGH. Data appears at the outputs (pins 1Y to 4Y) in true (non-inverting) form from the selected inputs. The 74LVC257A is the logic implementation of a 4-pole, 2-position switch, where the position of the switch is determined by the logic levels applied to pin S. The outputs are forced to a high-impedance OFF-state when pin $\overline{OE}$ is HIGH.

QUICK REFERENCE DATA

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $T_{amb} = 25$ °C.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nI0, nI1 to nY	$C_L = 50$ pF; $V_{CC} = 3.3$ V	2.9	ns
	propagation delay S to nY	$C_L = 50$ pF; $V_{CC} = 3.3$ V	3.2	ns
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to nY	$C_L = 50$ pF; $V_{CC} = 3.3$ V	3.7	ns
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to nY	$C_L = 50$ pF; $V_{CC} = 3.3$ V	3.2	ns
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per gate	$V_{CC} = 3.3$ V; notes 1 and 2		
		outputs enabled	16	pF
		outputs disabled	7.0	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz;
   f_o = output frequency in MHz;
   C_L = output load capacitance in pF;
   V_{CC} = supply voltage in Volts;
   N = total load switching outputs;
   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

FUNCTION TABLE

See note 1.

INPUT				OUTPUT
$\overline{OE}$	S	nI0	nI1	nY
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

Note

1. H = HIGH voltage level;
   L = LOW voltage level;
   X = don't care;
   Z = high-impedance OFF-state.

ORDERING INFORMATION

TYPE NUMBER	TEMPERATURE RANGE	PACKAGE			
		PINS	PACKAGE	MATERIAL	CODE
74LVC257AD	–40 to +125 °C	16	SO16	plastic	SOT109-1
74LVC257ADB	–40 to +125 °C	16	SSOP16	plastic	SOT338-1
74LVC257APW	–40 to +125 °C	16	TSSOP16	plastic	SOT403-1
74LVC257ABQ	–40 to +125 °C	16	DHVQFN16	plastic	SOT763-1

PINNING

PIN	SYMBOL	DESCRIPTION
1	S	common data select input
2	1I0	data input from source 0
3	1I1	data input from source 1
4	1Y	3-state multiplexer output
5	2I0	data input from source 0
6	2I1	data input from source 1
7	2Y	3-state multiplexer output
8	GND	ground (0 V)
9	3Y	3-state multiplexer output
10	3I1	data input from source 1
11	3I0	data input from source 0
12	4Y	3-state multiplexer output
13	4I1	data input from source 1
14	4I0	data input from source 0
15	$\overline{OE}$	3-state output enable input (active LOW)
16	V_{CC}	supply voltage

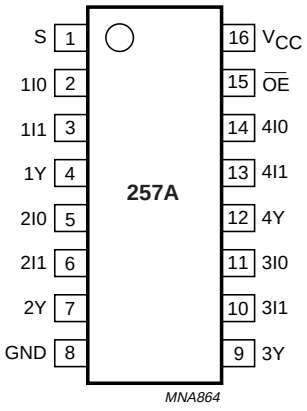
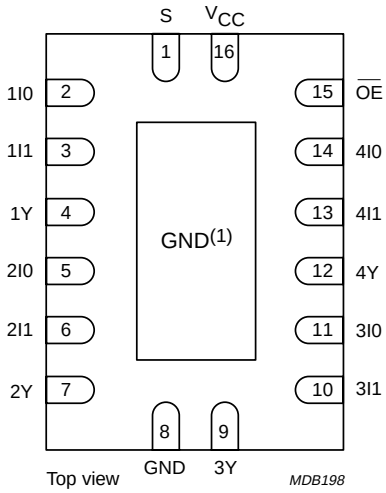


Fig.1 Pin configuration SO16 and (T)SSOP16.



(1) The die substrate is attached to this pad using conductive die attach material. It can not be used as a supply pin or input.

Fig.2 Pin configuration DHVQFN16.

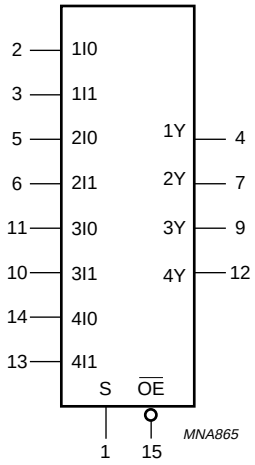


Fig.3 Logic symbol.

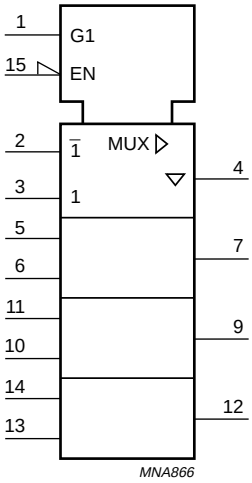


Fig.4 Logic symbol (IEEE/IEC).

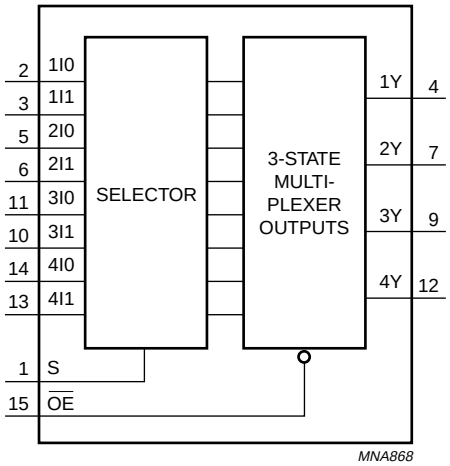


Fig.5 Functional diagram.

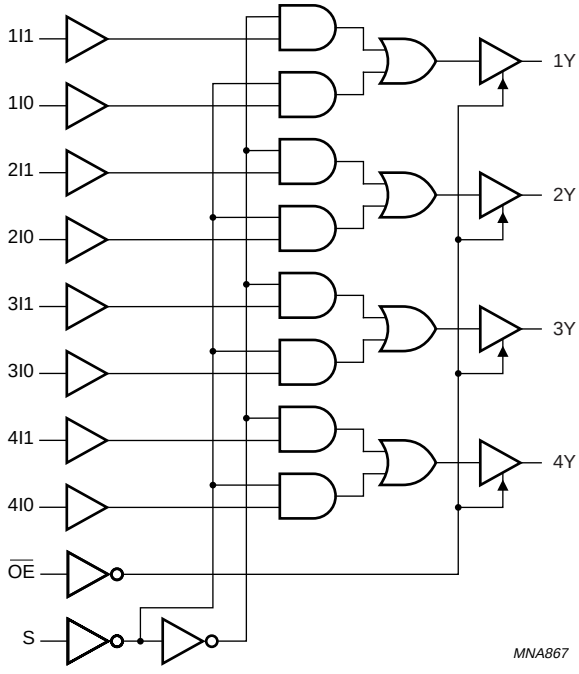


Fig.6 Logic diagram.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage	for maximum speed performance	2.7	3.6	V
		for low-voltage applications	1.2	3.6	V
V_I	input voltage		0	5.5	V
V_O	output voltage	HIGH or LOW state	0	V_{CC}	V
		3-state	0	5.5	V
T_{amb}	operating ambient temperature	in free air	–40	+125	°C
t_r, t_f	input rise and fall times	V_{CC} = 1.2 to 2.7 V	0	20	ns/V
		V_{CC} = 2.7 to 3.6 V	0	10	ns/V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+6.5	V
I_{IK}	input diode current	$V_I < 0$	–	–50	mA
V_I	input voltage	note 1	–0.5	+6.5	V
I_{OK}	output diode current	$V_O > V_{CC}$ or $V_O < 0$	–	±50	mA
V_O	output voltage	HIGH or LOW state; note 1	–0.5	V_{CC} + 0.5	V
		3-state; note 1	–0.5	+6.5	V
I_O	output source or sink current	V_O = 0 to V_{CC}	–	±50	mA
I_{CC}, I_{GND}	V_{CC} or GND current		–	±100	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	power dissipation	T_{amb} = –40 to +125 °C; note 2	–	500	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. For SO16 packages: above 70 °C derate linearly with 8 mW/K.
   For SSOP16 and TSSOP16 packages: above 60 °C derate linearly with 5.5 mW/K.
   For DHVQFN16 packages: above 60 °C derate linearly with 4.5 mW/K.

DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = −40 to +85 °C; note 1							
V_{IH}	HIGH-level input voltage		1.2	V_{CC}	–	–	V
			2.7 to 3.6	2.0	–	–	V
V_{IL}	LOW-level input voltage		1.2	–	–	GND	V
			2.7 to 3.6	–	–	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = −100 μA	2.7 to 3.6	V_{CC} − 0.2	V_{CC}[2]	–	V
		I_O = −12 mA	2.7	V_{CC} − 0.5	–	–	V
		I_O = −18 mA	3.0	V_{CC} − 0.6	–	–	V
		I_O = −24 mA	3.0	V_{CC} − 0.8	–	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 100 μA	2.7 to 3.6	–	GND[2]	0.2	V
		I_O = 12 mA	2.7	–	–	0.4	V
		I_O = 24 mA	3.0	–	–	0.55	V
I_{LI}	input leakage current	V_I = 5.5 V or GND	3.6	–	±0.1	±5	μA
I_{OZ}	3-state output OFF-state current	V_I = V_{IH} or V_{IL}; V_O = 5.5 V or GND	3.6	–	0.1	±5	μA
I_{off}	power-off leakage supply	V_I or V_O = 5.5 V	0.0	–	0.1	±10	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0	3.6	–	0.1	10	μA
ΔI_{CC}	additional quiescent supply current per pin	V_I = V_{CC} − 0.6 V; I_O = 0	2.7 to 3.6	–	5[2]	500	μA

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = −40 to +125 °C							
V_{IH}	HIGH-level input voltage		1.2	V_{CC}	–	–	V
			2.7 to 3.6	2.0	–	–	V
V_{IL}	LOW-level input voltage		1.2	–	–	0	V
			2.7 to 3.6	–	–	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = −100 μA	2.7 to 3.6	V_{CC} − 0.3	–	–	V
		I_O = −12 mA	2.7	V_{CC} − 0.65	–	–	V
		I_O = −18 mA	3.0	V_{CC} − 0.75	–	–	V
		I_O = −24 mA	3.0	V_{CC} − 1	–	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 100 μA	2.7 to 3.6	–	–	0.3	V
		I_O = 12 mA	2.7	–	–	0.6	V
		I_O = 24 mA	3.0	–	–	0.8	V
I_{LI}	input leakage current	V_I = 5.5 V or GND	3.6	–	–	±20	μA
I_{OZ}	3-state output OFF-state current	V_I = V_{IH} or V_{IL}; V_O = 5.5 V or GND	3.6	–	–	±20	μA
I_{off}	power-off leakage supply	V_I or V_O = 5.5 V	0.0	–	–	±20	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0	3.6	–	–	40	μA
ΔI_{CC}	additional quiescent supply current per pin	V_I = V_{CC} − 0.6 V; I_O = 0	2.7 to 3.6	–	–	5000	μA

Notes

1. All typical values are measured T_{amb} = 25 °C.
2. These typical values are measured at V_{CC} = 3.3 V.

AC CHARACTERISTICS

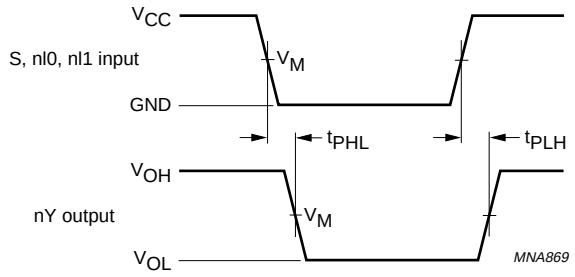
GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF; $R_L = 500\ \Omega$.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V_{CC} (V)				
T_{amb} = −40 to +85 °C; note 1							
t_{PHL}/t_{PLH}	propagation delay nI0, nI1 to nY	see Figs 7 and 9	1.2	–	16	–	ns
			2.7	1.0	3.0	5.4	ns
			3.0 to 3.6	1.0	2.9(2)	4.6	ns
	propagation delay S to nY	see Figs 7 and 9	1.2	–	18	–	ns
			2.7	1.0	3.6	7.5	ns
			3.0 to 3.6	1.0	3.2(2)	6.4	ns
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to nY	see Figs 8 and 9	1.2	–	15	–	ns
			2.7	1.5	3.6	6.7	ns
			3.0 to 3.6	1.0	3.7(2)	5.6	ns
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to nY	see Figs 8 and 9	1.2	–	8	–	ns
			2.7	1.5	3.1	4.7	ns
			3.0 to 3.6	1.0	3.2(2)	4.3	ns
$t_{sk(0)}$	skew	note 3	3.0 to 3.6	–	–	1.0	ns
T_{amb} = −40 to +125 °C							
t_{PHL}/t_{PLH}	propagation delay nI0, nI1 to nY	see Figs 7 and 9	1.2	–	–	–	ns
			2.7	1.0	–	7.0	ns
			3.0 to 3.6	1.0	–	6.0	ns
	propagation delay S to nY	see Figs 7 and 9	1.2	–	–	–	ns
			2.7	1.0	–	9.5	ns
			3.0 to 3.6	1.0	–	8.0	ns
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to nY	see Figs 8 and 9	1.2	–	–	–	ns
			2.7	1.5	–	8.5	ns
			3.0 to 3.6	1.0	–	7.0	ns
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to nY	see Figs 8 and 9	1.2	–	–	–	ns
			2.7	1.5	–	6.0	ns
			3.0 to 3.6	1.0	–	5.5	ns
$t_{sk(0)}$	skew	note 3	3.0 to 3.6	–	–	1.5	ns

Notes

1. All typical values are measured $T_{amb} = 25$ °C.
2. These typical values are measured at $V_{CC} = 3.3$ V.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

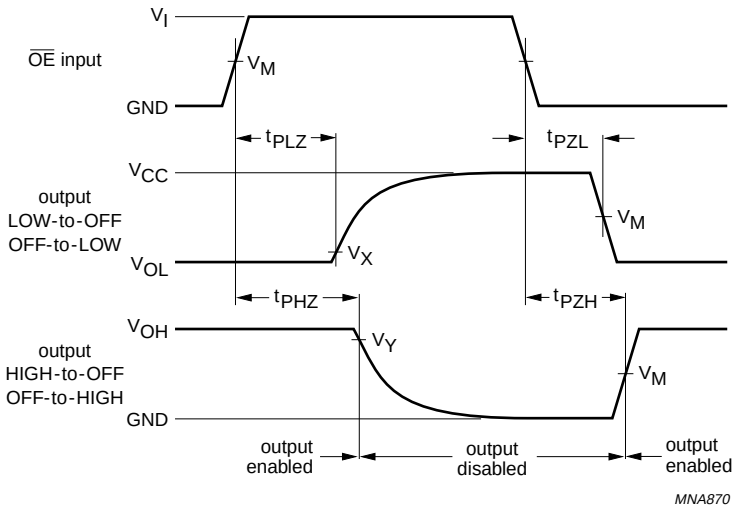
AC WAVEFORMS



V_{CC}	V_M	INPUT	
		V_I	$t_r = t_f$
1.2 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.5 ns
2.7 V	1.5 V	2.7 V	≤ 2.5 ns
3.0 to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.7 Input (S, nI0 and nI1) to output (nY) propagation delays.

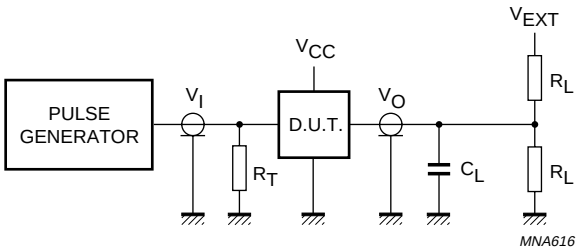


V_{CC}	V_M	INPUT	
		V_I	$t_r = t_f$
1.2 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.5 ns
2.7 V	1.5 V	2.7 V	≤ 2.5 ns
3.0 to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns

$V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V;
$V_X = V_{OL} + 0.1$ V at $V_{CC} < 2.7$ V;
$V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V;
$V_Y = V_{OH} - 0.1$ V at $V_{CC} < 2.7$ V.

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.8 3-state enable and disable times.



V_{CC}	V_I	C_L	R_L	V_{EXT}		
				t_{PLH}/t_{PHL}	t_{PZH}/t_{PHZ}	t_{PZL}/t_{PLZ}
1.2 V	V_{CC}	50 pF	500 Ω(1)	open	GND	$2 \times V_{CC}$
2.7 V	2.7 V	50 pF	500 Ω	open	GND	$2 \times V_{CC}$
3.0 to 3.6 V	2.7 V	50 pF	500 Ω	open	GND	$2 \times V_{CC}$

Note

1. The circuit performs better when R_L = 1000 Ω.

Definitions for test circuits:

R_L = Load resistor.

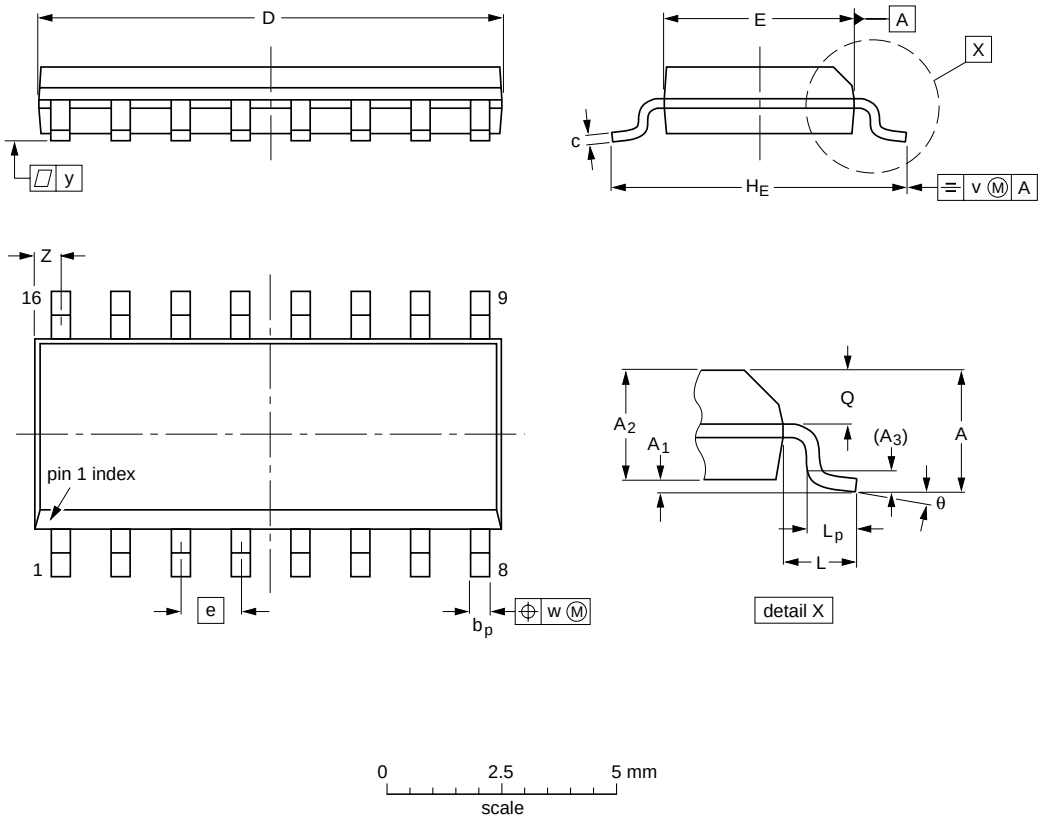
C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.9 Load circuitry for switching times.

PACKAGE OUTLINES

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

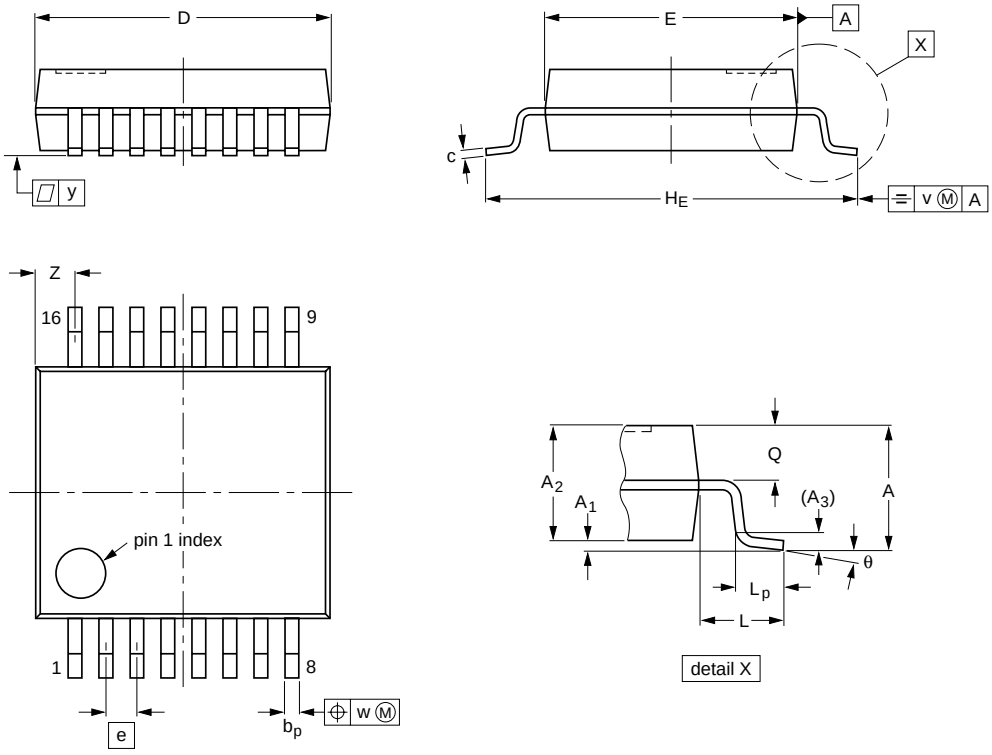
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



0 2.5 5 mm
scale

DIMENSIONS (mm are the original dimensions)

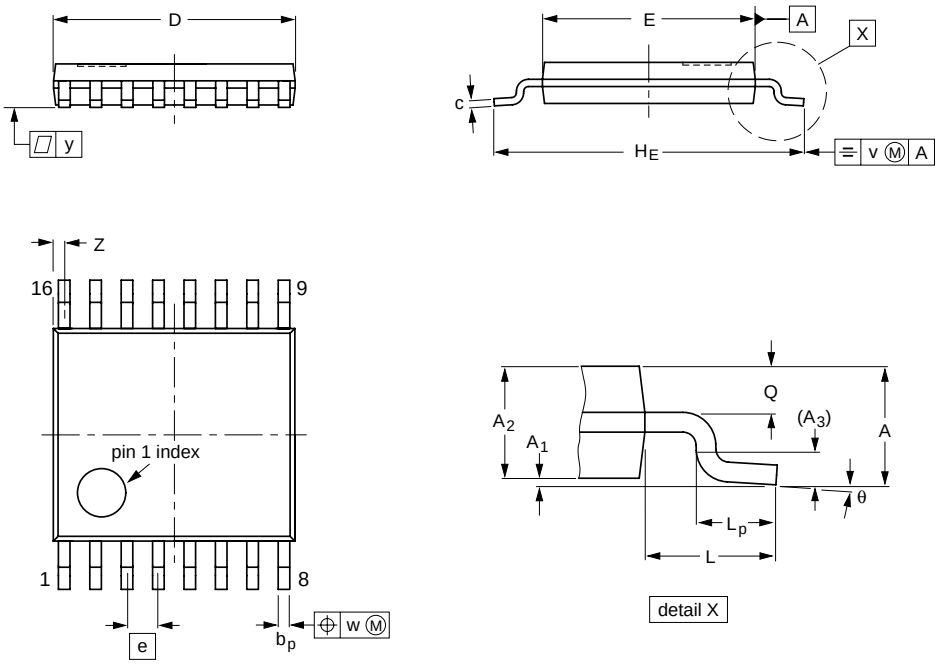
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8^o 0^o

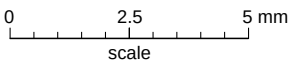
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT338-1		MO-150				~~99-12-27~~ 03-02-19

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**





DIMENSIONS (mm are the original dimensions)

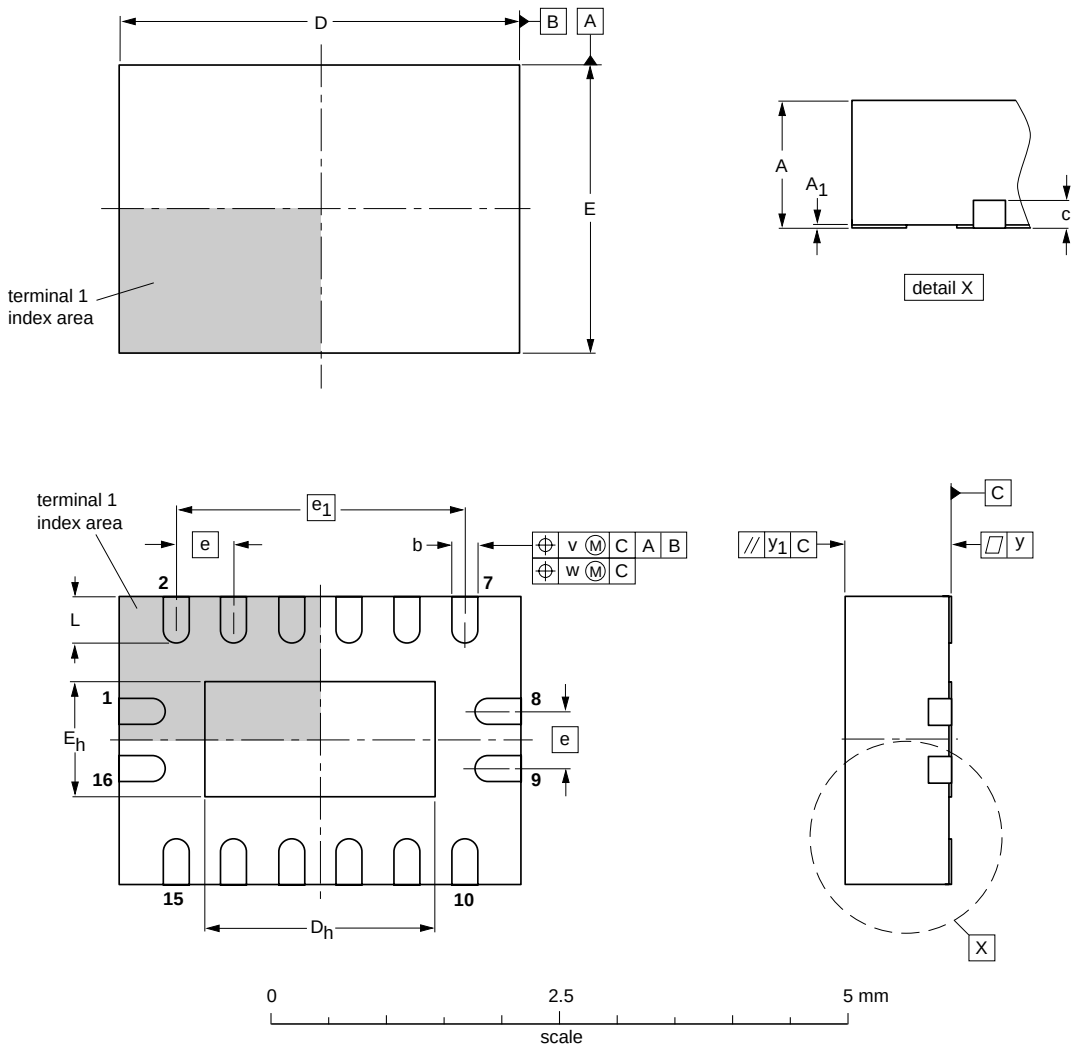
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm **SOT763-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.6 3.4	2.15 1.85	2.6 2.4	1.15 0.85	0.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT763-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Contact information

For additional information please visit **http://www.semiconductors.philips.com**. Fax: **+31 40 27 24825**
For sales offices addresses send e-mail to: **sales.addresses@www.semiconductors.philips.com**.

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